C1PE JC76
NOV 25 2002
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED

Applicant : ASAI Motoo et al.
Application No. : 09/319,258
I.A. Filed : December 18, 1997
For : PRINTED WIRING BOARD AND METHOD FOR MANUFACTURING THE SAME

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington D.C. 20231

Sirs:

Yoshikazu KASAI, of #906, 7-19, Tsurugamine 2-Chome, Asahi-Ku, Yokohama-Shi, Kanagawa, 241-0022 Japan
declares:

(1) that I know well both the Japanese and English languages;

(2) that I have translated the Japanese Patent Application No. 9-197526 from Japanese to English;

(3) that the attached English translation is a true and correct translation of the Japanese Patent Application No. 9-197526 to the best of my knowledge and belief; and

(4) that all statements made of my own knowledge are true and that all statements made of information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such false statement may jeopardize the validity of the application or any patent issuing thereon.

October 21, 2002

Yoshikazu Kasai

Translator: Yoshikazu KASAI

English Translation
Japanese Patent Application No. 9-197526

[Identification of the Document] Patent Application
[Reference Number] H09OGAD025
[Date of Submission] July 23, 1997
[Addressee] Director-General of the Patent Office
ARAI Hisamitsu
[International Patent Classification] H05K 3/00
[Title of Invention]
MULTILAYER PRINTED CIRCUIT BOARD AND METHOD OF PRODUCING THE SAME
[Number of Claims] 7
[Inventor(s)]
[Address]
c/o IBIDEN Co., Ltd. 1-1, Kitakata, Ibigawa-cho, Ibi-gun, Gifu
[Name] ASAI Motoo
[Applicant(s)]
[Identification Number] 000000158
[Name] IBIDEN Co., Ltd.
[Representative]
[Identification Number] 100080687
[Postal Code] 104
[Patent Attorney]
[Name] OGAWA Junzo
[Telephone Number] 03-3561-2211
[Other Representative]
[Identification Number] 100077126
[Patent Attorney]
[Name] NAKAMURA Morio
[Priority Claim based on Prior Application(s)]
[Application Number] 8-354971
[Filing Date] December 19, 1996
[Priority Claim based on Prior Application(s)]
[Application Number] 8-357801
[Filing Date] December 28, 1996
[Indication of Fee]
[Deposit Account Number] 011947
[Amount of Payment] 21000
[List of Attached Items]
[Identification of Item] 1 Copy of Specification
[Identification of Item] 1 Copy of Drawings
[Identification of Item] 1 Copy of Abstract
[General Authorization Number] 9704370

[Identification of the Document]
Specification

[Title of the Invention]
Multilayer Printed Circuit Board and Method of Producing the Same

[Scope of Claims for Patent]

[Claim 1]
A multilayer printed circuit board wherein a conductor circuit layer is formed on a substrate and an interlaminar insulating layer is formed on the conductor circuit layer, characterized in that
the conductor circuit layer is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit.

[Claim 2]
A multilayer printed circuit board wherein an interlaminar insulating layer is formed on a substrate having formed thereon a conductor circuit layer, characterized in that
the conductor circuit layer is comprised of an electroless plated film and an electrolytic plated film, and
the conductor circuit layer is provided with a roughened layer on at least a part of the surface thereof.

[Claim 3]
A multilayer printed circuit board according to claim 1 or 2, wherein the conductor circuit layer is provided with a roughened layer on at least a part of the surface inclusive of a side face thereof.

[Claim 4]
A multilayer printed circuit board according to claim 1 or 2, wherein the conductor circuit layer is provided with a roughened layer on at least a part of the side face thereof.

[Claim 5]
A multilayer printed circuit board according of any one of claims 1~4, wherein the roughened layer is made of a copper-nickel-phosphorus alloy plating layer.

[Claim 6]
A method of producing a multilayer printed circuit board comprising steps of:
subjecting a substrate to an electroless plating,
forming a plating resist thereon,

subjecting the substrate to an electrolytic plating,
removing the plating resist,
forming a conductor circuit layer comprised of the electroless plated film and the electrolytic plated film by etching,
further forming a roughened layer on at least a part of the surface of the conductor circuit; and then
forming an interlaminar insulating layer.

[Claim 7]
A method of producing a multilayer printed circuit board according to claim 6, wherein the roughened layer is formed by a copper-nickel-phosphorus alloy plating.

[Detailed Explanation of the Invention]
[0001]
[Technical Field where the Invention belongs to]
The invention relates to a multilayer printed circuit board and a method of producing the same, and more particularly to a multilayer printed circuit board which can control the occurrence of cracks in the heat cycle without the degradation of peel strength, and a method of producing the same.

[0002]
[Prior Art]
Recently, the so-called build-up multilayer wiring boards are in demand for high densification of multilayer wiring boards. This build-up multilayer wiring board is produced, for example, by a method as described in JP-B-4-55555. That is, an insulating agent composed of a photosensitive adhesive for electroless plating is applied onto a core substrate, dried, exposed to a light and developed to form an interlaminar insulating layer having openings for viaholes, and then the surface of the interlaminar insulating layer is roughened by treating with an oxidizing agent or the like, and a plating resist is formed on the roughened surface, and thereafter a non-forming portion of the plating resist is subjected to an electroless plating to form viaholes and conductor circuits, and then such steps are repeated plural times to obtain a build-up multilayer wiring board.

[0003]
[Problem to be solved by the Invention]
However, in the thus obtained multilayer printed circuit board, the conductor circuit is formed on the non-forming portion of the plating resist and the plating resist remains in the inner layer as it is.
Therefore, if IC chips are mounted on such a wiring board, there is a problem that warping of the board is caused by a

difference of a thermal expansion coefficient between the IC chip and the insulating resin layer in the heat cycle to concentrate stress into a boundary portion between the plating resist and the conductor circuit due to poor adhesion property therebetween and hence cracks are generated in the interlaminar insulating layer contacting with the boundary portion.

[0004]

It is, therefore, an object of the invention to solve the aforementioned problems of the conventional technique.

It is a main object of the invention to prevent cracks of the interlaminar insulating layer created in the heat cycle without degrading other properties, particularly peel strength.

[0005]

[Means for solving the Problem]

The inventor has made various studies in order to achieve the above objects and as a result, the invention lying in the following structure has been accomplished.

(1) The multilayer printed circuit board according to the invention has a conductor circuit layer formed on a substrate and an interlaminar insulating layer formed on the conductor circuit layer, which is characterized in that

the conductor circuit layer is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit layer.

Moreover, in the multilayer printed circuit board, the conductor circuit layer is preferably provided with a roughened layer on at least a part of the surface inclusive of a side surface thereof, and the roughened layer is preferably a plated layer of copper-nickel-phosphorus alloy.

[0006]

(2) A method of producing a multilayer printed circuit board according to the invention is characterized by the steps of:

subjecting a substrate to an electroless plating;

forming a plating resist thereon;

subjecting the substrate to an electrolytic plating;

removing the plating resist;

forming a conductor circuit layer comprised of the electroless plated film and the electrolytic plated film by etching;

further forming a roughened layer on at least a part of the surface of the conductor circuit layer; and then

forming an interlaminar insulating layer.

Moreover, the roughened layer is preferably formed by the

plating of copper-nickel-phosphorus alloy.

[0007]
[Mode for carrying out the Invention]
The printed circuit board according to the invention lies in that the conductor circuit layer is comprised of an electrolytic plated film and an electroless plated film, and the electroless plated film is located at an inner layer side and the electrolytic plated film is located at an outer layer side (see enlarged views of Fig. 18 and Fig. 19). In such a structure, since the electrolytic plated film is softer and more malleable than the electroless plated film, the conductor circuit layer is able to comply with size change of the interlaminar insulating resin layer even if warping of the substrate is generated in the heat cycle.
Moreover, in the printed circuit board according to the invention, since the roughened layer is formed on the surface of the conductor circuit layer, the conductor circuit layer is strongly adhered to the interlaminar insulating resin layer and is capable of being easily complied with a change in size of the interlaminar insulating resin layer.

[0008]
As a result, even when an IC chip is mounted on the printed circuit board according to the invention and subjected to a heat cycle test under -55℃~125℃, generation of cracks in the interlaminar insulating resin layer starting from the conductor circuit can be prevented, and also the peeling is not observed.
Particularly, the provision of the roughened layer formed on at least a part of the side face of the conductor circuit is advantageous in a point that generation of cracks in the interlaminar insulating resin layer starting from the boundary between the side face of the conductor circuit and the interlaminer resin contacting therewith can be prevented.

[0009]
Moreover, in the printed circuit board according to the invention, the inner layer side of the conductor is constituted with the electroless plated film harder than the electrolytic plated film, and hence the peel strength is never lowered. Because the higher the hardness of the portion which is in contact with an interlaminar insulating layer (in case of adopting an adhesive for electroless plating as described later as an interlaminar insulating layer, the portion which is contact with a roughened surface), the higher the peel strength becomes.

[0010]
Such a multilayer printed circuit board can easily be

produced according to the invention.

[0011]

Moreover, JP-A-6-283860 discloses a technique of removing the plating resist in the inner layer and providing a roughened layer of copper-nickel-phosphorus on the surface of the conductor circuit composed of an electroless plated film to prevent interlaminar peeling. However, there is no understanding about cracks caused when the heat cycle test is actually carried out after the mounting of IC chips, and only a conductor circuit composed of only an electroless plated film is disclosed. Moreover, when a supplementary test of the heat cycle at -55℃~125℃ is carried out (see Comparative Example), cracking is not observed in about 1000 cycles, but when the cycle number exceeds 1000 cycles, cracking is observed. Therefore, this invention is entirely different from the present invention.

[0012]

In the invention, it is desirable that the roughened layer formed on the surface of the conductor circuit is a roughened surface of copper formed by an etching treatment, a polishing treatment, an oxidation treatment or a redox treatment, or a roughened surface of a plated film formed by subjecting to a plating treatment.

[0013]

Particularly, it is desirable that the roughened layer is an alloy layer composed of copper-nickel-phosphorus. Because the alloy layer is a needle-shaped crystal layer and is excellent in the adhesion property to the solder resist layer. Further, even if a solder body is formed on the alloy layer, the electrical conductivity is not largely changed, and hence the solder body can be formed on the metal pad.

The composition of the alloy layer is desirable to be 90~96 wt% of copper: 1~5 wt% of nickel and 0.5~2 wt% of phosphorus because the needle-shaped structure is obtained in such a composition ratio.

[0014]

Moreover, when a composition of Cu-Ni-P alloy capable of forming the needle-shaped crystal is shown in a triangular diagram of three components, it becomes as Fig. 20. In this figure, the range surrounded by (Cu, Ni, P)=(100, 0, 0), (90, 10, 0), (90, 0, 10) is preferable.

[0015]

When the roughened layer is formed by the oxidation

treatment, it is desirable to use a solution of an oxidizing agent comprising sodium chlorite, sodium hydride and sodium phosphate.

When the roughened layer is formed by the redox treatment, it is desirably carried out by immersing in a solution of a reducing agent comprising sodium hydroxide and sodium borohydride after the above oxidation treatment.

[0016]

The roughened layer formed on the surface of the conductor circuit layer desirably has a thickness of 1~5 μm. Because, if the thickness is too small, the roughened layer itself is apt to be damaged and peeled, while if it is too thin, adhesion is lowered.

[0017]

In the invention, the electroless plated film constituting the conductor circuit layer desirably has a thickness of 0.1~5 μm, preferably 0.5~3 μm. Because, if the thickness is too small, the ability to follow the interlaminar insulating resin layer lowers, while if it is too thin, degradation of peel strength is caused and electric resistance becomes large in the case of being subjected to an electrolytic plating to cause scattering in the thickness of the plated film.

[0018]

Furthermore, the electrolytic plated film constituting the conductor circuit layer desirably has a thickness of 5~30 μm, preferably 10~20 μm. Because, if the thickness is too small, degradation of peel strength is caused, while if it is too thin, the ability to follow the interlaminar insulating resin layer lowers.

[0019]

In the invention, it is desirable to form the roughened layer on at least a side face of the conductor circuit layer. Because, cracks generated in the interlaminar insulating resin layer due to the heat cycle will result from the bad adhesion between the side face of the conductor circuit layer and the insulating resin layer, but in such a structure, generation of cracks in the interlaminar insulating resin layer starting from the boundary between the side face of the conductor circuit and the insulating resin layer can be prevented.

[0020]

In the invention, it is desirable that the adhesive for electroless plating is used as the interlaminar insulating resin layer constituting the above wiring substrate. The adhesive for electroless plating is optimum to be obtained by dispersing cured

heat-resistant resin particles soluble in acid or oxidizing agent into an uncured heat-resistant resin hardly soluble in acid or oxidizing agent through curing.

Because, the heat-resistant resin particles can be dissolved and removed by treating with an acid or an oxidizing agent to form a roughened surface of octopus-trap shaped anchors on its surface.

[0021]

In the adhesive for electroless plating, the cured heat-resistant resin particles are desirable to be selected from ① heat-resistant resin powder having an average particle size of not more than 10 μm, ② aggregated particles formed by aggregating heat-resistant resin powder having an average particle size of not more than 2 μm, ③ a mixture of heat-resistant resin powder having an average particle size of 2~10 μm and heat-resistant resin powder having an average particle size of not more than 2 μm, ④ false particles formed by adhering at least one of heat-resistant resin powder and inorganic powder having an average particle size of not more than 2 μm onto the surface of heat-resistant resin powder having an average particle size of 2~10 μm, and ⑤ a mixture of heat-resistant resin powder having an average particle size of 0.1~0.8 μm and heat-resistant resin powder having an average particle size of more than 0.8 μm but less than 2 μm. Because they can form more complicated anchor.

[0022]

Next, a method of producing the printed circuit board according to the invention will be explained.

(1) At first, a wiring substrate is prepared by forming an inner layer copper pattern on the surface of a core substrate.

The core pattern of the wiring substrate is formed by a method of etching a copper-clad laminate, or a method of forming an adhesive layer for electroless plating on a substrate such as glass epoxy substrate, polyimide substrate, ceramic substrate, metal substrate or the like and roughening the surface of the adhesive layer and subjecting the roughened surface to an electroless plating.

[0023]

If necessary, a roughened layer of copper-nickel-phosphorus alloy is further formed on the copper pattern surface of the wiring substrate.

The roughened layer is formed by the electroless plating. The composition of the electroless plating aqueous solution is desirable to have a copper ion concentration of 2.2×10^{-2}~4.1×10^{-2}

mol/l, a nickel ion concentration of 2.2×10^{-3} ~4.1×10^{-3} and a hypophosphorus acid ion concentration of 0.20~0.25 mol/l.

The film deposited within the above range is needle in the crystal structure and is excellent in the anchor effect. The electroless plating bath may be added with a complexing agent and additives in addition to the above compounds.

As a method of forming the roughened layer, there are oxidation-reduction (blackening)-reduction treatment, a method of etching the copper surface along a grain boundary to form a roughened layer and the like.

[0024]

Moreover, through-holes are formed in the core substrate, and the front and back wiring layers may electrically be connected to each other through the through-holes.

And also, a resin may be filled in the through-holes and between the conductor circuits of the core substrate to ensure the smoothness thereof (see Fig. 1~Fig. 4).

[0025]

(2) Then, an interlaminar insulating resin layer is formed on the wiring substrate prepared in step (1).

In the invention, it is particularly desirable to use an adhesive for electroless plating as the interlaminar insulating resin material (see Fig. 5).

[0026]

(3) After the adhesive layer for electroless plating formed in step (2) is dried, an opening portion for the formation of viahole is formed, if necessary.

The opening portion for the formation of viahole is formed in the adhesive layer by light exposure, development and thermosetting in case of the photosensive resin, or by thermosetting and laser working in case of the thermosetting resin (see Fig. 6).

[0027]

(4) Then, epoxy resin particles existing on the surface of the cured adhesive layer are dissolved and removed with an acid or an oxidizing agent to roughen the surface of the adhesive layer (see Fig. 7).

Here, as the acid, there are phosphoric acid, hydrochloric acid, sulfuric acid, and an organic acid such as formic acid, acetic acid or the like, and particularly, the use of the organic acid is desirable. Because, when it hardly corrodes the metal conductor layer exposed from the viahole by the roughening treatment.

On the other hand, as the oxidizing agent, it is desirable to use chromic acid, permanganese (potassium permanganese or

the like) and so on.

[0028]
(5) Then, a catalyst nucleus is applied to the wiring substrate provided with the roughened surface of the adhesive layer.

In the application of the catalyst nucleus, it is desirable to use a noble metal ion, a noble metal colloid or the like, and in general, palladium chloride or palladium colloid is used. Moreover, it is desirable to conduct a heating treatment for fixing the catalyst nucleus. As the catalyst nucleus, palladium is favorable.

[0029]
(6) Then, the surface of the adhesive layer for electroless plating is subjected to an electroless plating to form an electroless plated film on the whole of the roughened surface (see Fig. 8). In this case, the thickness of the electroless plated film is 0.1~5 μm, more preferably 0.5~3 μm.

Then, a plating resist is formed on the electroless plated film (see Fig. 9). As the plating resist composition, it is particularly desirable to use a composition comprised of an imidazole curing agent and an acrylate of cresol type epoxy resin, phenol novolac type epoxy resin or the like, but use may be made of commercially available products.

[0030]
(7) Then, a portion not forming the plating resist is subjected to an electrolytic plating to form conductor circuits and viaholes (see Fig. 10). In this case, it is desirable that the thickness of the electrolytic plated film is 5~30 μm.

Here, as the electrolytic plating, it is desirable to use an electrolytic copper plating.

[0031]
(8) Moreover, after the plating resist is removed, the electroless plated film beneath the plating resist is removed by dissolving in an etching solution such as a mixture of sulfuric acid and hydrogen peroxide, sodium persulfate, ammonium persulfate or the like to obtain an independent conductor circuit (see Fig. 11).

[0032]
(9) Then, a roughened layer is formed on the surface of the conductor circuit (see Fig. 12).

As a method of forming the roughened layer, there are etching treatment, polishing treatment, redox treatment and plating treatment.

Among these treatments, the redox treatment is conducted by using an oxidation bath (blackening bath) of NaOH

(10 g/l), $NaClO_2$ (40 g/l) and Na_2PO_4 (6 g/l) and a reduction bath of NaOH (10 g/l) and $NaBH_4$ (5 g/l).

Furthermore, the roughened layer made from copper-nickel-phosphorus alloy layer is formed by deposition through electroless plating.

As the electroless alloy plating aqueous solution, it is favorable to use a plating bath of aqueous solution composition comprising copper sulfate: 1~40 g/l, nickel sulfate: 0.1~6.0 g/l, citric acid: 10~20 g/l, hypophosphite: 10~100 g/l, boric acid: 10~40 g/l and surfactant: 0.01~10 g/l.

[0033]

(10) Then, an adhesive layer for electroless plating as an interlaminar insulating resin layer is formed on the substrate (see Fig. 13).

(11) Moreover, an upper layer conductor circuit layer is formed by repeating steps (3)~(8) (see Figs. 14~17). Furthermore, here, a roughened layer may be formed on the surface of the conductor circuits in the same manner as in step (9).

[0034]

(12) Then, a solder resist composition is applied onto both surfaces of the thus obtained wiring substrate and the coating film of the solder resist composition is dried, then, a photomask film depicted with an opening portion is placed on the dried film, which is subjected to light exposure and developing treatments to form an opening portion exposing a pad portion of the conductor circuit. Here, the opening size of the opening portion can be made larger than the diameter of the pad to completely expose the pad. Or the opening size of the opening portion can be made smaller than the diameter of the pad so as to cover the peripheral edge of the pad with the solder resist. In this case, the pad can be restrained by the solder resist to prevent the peeling of the pad.

[0035]

(13) Then, a metal layer of "nickel-gold" is formed on the pad portion exposed from the opening portion.

[0036]

(14) Then, a solder body is fed onto the pad portion exposed from the opening portion.

As a method of feeding the solder body, use may be made of a solder transferring method and a solder printing method. Here, the solder transferring method is a method wherein a solder foil is attached to a prepreg and etched so as to leave only a portion corresponding to the opening portion to render into a solder carrier film having a solder pattern, and the solder carrier film is

laminated so as to contact the solder pattern with the pad after a flux is applied to the opening portion in the solder resist of the substrate and heated to transfer the solder onto the pad. On the other hand, the solder printing method is a method wherein a metal mask having through-holes corresponding to the pads is placed onto the substrate and a solder paste is printed and heated.

[0037]
[Examples]
(Example 1)
(1) As a starting material, there is used a copper-clad laminate obtained by laminating a copper foil 8 of 18 μm on each surface of a substrate1 made from a glass epoxy resin or BT (bismaleimide-triazine) resin having a thickness of 0.6 mm (see Fig. 1) The copper-clad laminate is etched in a pattern according to the usual manner, which is pierced and subjected to an electroless plating to form inner layer copper pattern 4 and through-holes 9 on both surfaces of the substrate (see Fig. 2).

Further, bisphenol F-type epoxy resin is filled between the conductor circuits 4 and the through-holes 9 (see Fig. 3).

[0038]
(2) The substrate treated in step (1) is washed with water, dried, acidicly degreased and soft-etched, then, the substrate is treated with a catalyst solution comprising palladium chloride and organic acid to give a Pd catalyst, which is activated and subjected to a plating in an electroless plating bath comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having pH=9 to form a roughened layer 11 (uneven layer) of Cu-Ni-P alloy having a thickness of 2.5 μm on the surface of the copper conductor circuit 4 (see Fig. 4).

[0039]
(3) A photosensitive adhesive solution (interlaminar resin insulating agent) is prepared by mixing 70 parts by weight of 25% acrylated product of cresol novolac epoxy resin (made by Nippon Kayaku Co., Ltd., molecular weight: 2500) dissolved in DMDG (diethylene glycol dimethyl ether), 30 parts by weight of polyether sulphone (PES), 4 parts by weight of an imidazole curing agent (made by Shikoku Kasei Co., Ltd., trade name: 2E4MZ-CN), 10 parts by weight of caprolacton-modified tris(acroxyethyl) isocyanurate (made by Toa Gosei Co., Ltd, trade name: Aronix M325) as a photosensitive monomer, 5 parts by weight of benzophenone (made by Kanto Kagaku Co., Ltd) as a photoinitiator, 0.5 part by weight of Michelers' ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and 35 parts by weight at 5.5 μm on

average and 5 parts by weight at 0.5 μm on average of epoxy resin particles, adding NMP (normal methyl pyrolidone), adjusting a viscosity to 12 Pa·s in a homodisper aditating machine and kneading them through three holes.

[0040]
(4) The photosensitive adhesive solution obtained in step (3) is applied onto both surfaces of the substrate treated in step (2) by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60℃ for 30 minutes to form an adhesive layer 2 having a thickness of 60 μm (see Fig. 5).
(5) A photomask film depicted with viaholes is adhered onto each surface of the substrate provided with the adhesive layer 2 in step (4) and exposed by irradiation of ultraviolet rays.

[0041]
(6) The exposed substrate is developed by spraying DMTG (triethylene glycol dimethylether) solution to form openings for viaholes of 100 μm ϕ in the adhesive layer. Further, the substrate is exposed to a superhigh pressure mercury lamp at 3000 mJ/cm^2 and then heated at 100℃ for 1 hour, and thereafter at 150℃ for 5 hours to form an adhesive layer 2 of 50 μm in thickness having the openings (opening 6 for the formation of viahole) with an excellent size accuracy corresponding to the photomask film by the assembly of three (see Fig. 6). Moreover, the roughened layer 11 is partially exposed in the opening 6 for the viahole.

[0042]
(7) The substrate provided with the openings 6 for the viahole in steps (5), (6) is immersed in chromic acid for 2 minutes to dissolve and remove epoxy resin particles from the surface of the adhesive layer, whereby the surface of the adhesive layer is roughened. Thereafter, it is immersed in a neutral solution (made by Shipley) and washed with water (see Fig. 7).
(8) A palladium catalyst (made by Atotech Co., Ltd.) is applied to the substrate subjected to a roughened treatment (roughening depth: 5 μm) in step (7) to give a catalyst nucleus to the surface of the adhesive layer 2 and the opening 6 for the viahole.

[0043]
(9) The substrate is immersed in an electroless copper plating bath having the following composition to form an electroless copper plated film 12 having a thickness of 3 μm over the full roughened surface (see Fig. 8).
[Electroless plating aqueous solution]

EDTA	150 g/l

copper sulfate	20 g/l
HCHO	30 ml/l
NaOH	40 g/l
α, α'-bipyridyl	80 mg/l
PEG	0.1 g/l

[Electroless plating condition]
liquid temperature of 70℃ for 30 minutes

[0044]
(19) A commercially available photosensitive dry film is attached to the electroless copper plated film 12 formed in step (9) and a photomask film is placed on the dry film, which is exposed to a light at 100 mJ/cm^2 and developed with a solution of 0.8% sodium carbonate to form a plating resist 3 having a thickness of 15 μm (see Fig. 9).

[0045]
(11) Then, an electrolytic copper plated film 13 having a thickness of 15 μm is formed by applying an electrolytic copper plating under the following conditions (see Fig. 13).

[Electrolytic plating aqueous solution]

sulfuric acid	180 g/l
copper sulfate	80 g/l
additive (made by Atotech Japan Co., Ltd., trade name: Capalacido GL)	1 ml/g

[Electrolytic plating condition]

current density	1 A/dm^2
time	30 minutes
temperature	room temperature

[0046]
(12) After the plating resist 3 is peeled and removed with 5% KOH, the electroless plated film 12 beneath the plating resist 3 is dissolved and removed by etching with a mixed solution of sulfuric acid and hydrogen peroxide to form a conductor circuit 5 (including viaholes) of 18 μm in thickness comprised of the electroless copper plated film 12 and the electrolytic copper plated film 13 (see Fig. 11).

[0047]
The substrate provided with the conductor circuits 5 is immersed in an electroless plating aqueous solution comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant and having pH=9 to form a roughened layer 11 of copper-nickel-phosphorus having a thickness of 3 μm on the

surface of the conductor circuit 5 (see Fig. 12). When the roughened layer 11 is analyzed by EPMA (electro probe micro analyzer), it shows a composition ratio of Cu: 98 mol%, Ni: 1.5 mol% and P: 0.5 mol%.

[0048]
(14) Steps (4)~(12) are repeated to further obtain a wiring substrate formed with an upper layer conductor circuit (see Figs. 13~17).

[0049]
(15) On the other hand, a solder resist composition is prepared by mixing 46.67 g of a photosensitized oligomer (molecular weight: 4000) in which 50% of epoxy group in 60% by weight of cresol epoxy resin (made by Nippon Kayaku Co., Ltd.) dissolved in DMDG is acrylated, 15.0 g of 80% by weight of bisphenol A epoxy resin (made by Yuka Shell Co., Ltd., trade name: Epikote 1001) dissolved in methyl ethyl ketone, 1.6 g of an imidazole curing agent (made by Shikoku Kasei Co., Ltd., trade name: 2E4MZ-CN), 3 g of a polyvalent acrylic monomer (made by Nippon Kayaku Co., Ltd., trade name: R604) as a photosensitive monomer, 1.5 g of a polyvalent acrylic monomer (made by Kyoeisha Kagaku Co., Ltd., trade name: DPE6A), 0.71 g of a dispersion type defoaming agent (made by Sannopuko Co., Ltd., trade name: S-65), 2 g of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator and 0.2 g of Micheler's ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and adjusting a viscosity to 2.0 Pa·s at 25℃.

Moreover, the measurement of the viscosity is carried out by means of a B-type viscometer (made by Tokyo Keiki Co., Ltd., DVL-B model) with a rotor No. 4 in case of 60 rpm or a rotor No. 3 in case of 6 rpm.

[0050]
(16) The solder resist composition is applied onto the wiring substrate obtained in step (4) at a thickness of 20 μm. Then, the substrate is dried at 70℃ for 20 minutes and at 70℃ for 30 minutes and a photomask film is placed thereon and then exposed to an ultraviolet ray at 1000 mJ/cm^2 and developed with DMTG. Further, it is heated at 80℃ for 1 hour, at 100℃ for 1 hour, at 120℃ for 1 hour and at 150℃ for 3 hours to form a solder resist layer (thickness: 20 μm) opened in the pad portion (opening size: 200 μm).

[0051]
(17) Then, the substrate provided with the solder resist layer is immersed in an electroless nickel plating solution of pH=5

comprising 30 g/l of nickel chloride, 10 g/l of sodium hypophosphite and 10 g/l of sodium citrate for 20 minutes to form a nickel plated layer having a thickness of 5 μm in the opening portion. Further, the substrate is immersed in an electroless gold plating solution comprising 2 g/l of potassium gold cyanide, 75 g/l of ammonium chloride, 50 g/l of sodium citrate and 10 g/l of sodium hypophosphite at 93℃ for 23 seconds to form a gold plated layer having a thickness of 0.03 μm on the nickel plated layer.

[0052]
(18) Then, a solder paste is printed on the opening portion of the solder resist layer and reflowed at 200℃ to form solder bumps, whereby there is produced a printed circuit board having solder bumps.

[0053]
(Example 2)
A printed circuit board having solder bumps is produced in the same manner as in Example 1 except that the roughening of the surface of the conductor circuit is carried out by etching. In this case, an etching solution of "Durabond" made by Meck Co., Ltd. is used.

[0054]
(Example 3)
A. Preparation of an adhesive composition for electroless plating
① 35 parts by weight of a resin solution obtained by dissolving 25% acrylated product of cresol novolac epoxy resin (made by Nippon Kayaku Co, Ltd. molecular weight: 2500) in DMDG at a concentration of 80 wt% is mixed with 3.15 parts by weight of a photosensitive monomer (made by Toa Gosei Co., Ltd., trade name: Aronix M315), 0.5 part by weight of a defoaming agent (made by Sannopuko Co., Ltd., trade name: S-65) and 3.6 parts by weight of NMP with stirring.
② 12 parts by weight of polyether sulphone (PES) is mixed with 7.2 parts by weight at 1.0 μ m on average and 3.09 parts by weight at 0.5 μ m on average of epoxy resin particles (made by Sanyo Kasei Co, Ltd. trade name: Polymerpole) and further added with 30 parts by weight of NMP and mixed in a beads mill with stirring.
③ 2 parts by weight of an imidazole curing agent (made by Shikoku Kasei Co, Ltd. trade name: 2E-4MZ-CN) is mixed with 2 parts by weight of a photoinitiator (made by Ciba Geigey, trade name: Irgaquar I-907), 0.2 part by weight of a photosensitizer (made by Nippon Kayaku Co., Ltd., trade name: DETX-S) and 1.5 parts by weight of NMP with stirring.
These mixtures are mixed to prepare an adhesive

composition for electroless plating.

[0055]
B. Preparation of an under layer interlaminar insulating resin material

① 35 parts by weight of a resin solution obtained by dissolving 25% acrylated product of cresol novolac epoxy resin (made by Nippon Kayaku Co, Ltd. molecular weight: 2500) in DMDG at a concentration of 80 wt% is mixed with 4 parts by weight of a photosensitive monomer (made by Toa Gosei Co., Ltd., trade name: Aronix M315), 0.5 part by weight of a defoaming agent (made by Sannopuko Co., Ltd., trade name: S-65) and 3.6 parts by weight of NMP with stirring.

② 12 parts by weight of polyether sulphone (PES) is mixed with 14.49 parts by weight at 0.5 μm on average of epoxy resin particles (made by Sanyo Kasei Co, Ltd. Trade name: Polymerpole) and further added with 30 parts by weight of NMP and mixed in a beads mill with stirring.

③ 2 parts by weight of an imidazole curing agent (made by Shikoku Kasei Co, Ltd. trade name: 2E-4MZ-CN) is mixed with 2 parts by weight of a photoinitiator (made by Ciba Geigey, trade name: Irgaquar I-907), 0.2 part by weight of a photosensitizer (made by Nippon Kayaku Co., Ltd., trade name: DETX-S) and 1.5 parts by weight of NMP with stirring.

These mixtures are mixed to prepare a resin composition used as an underlayer side insulating layer constituting the interlaminar insulating resin layer of two-layer structure.

[0056]
C. Preparation of a resin filler

① 100 parts by weight of bisphenol F epoxy monomer (made by Yuka Shell Co, Ltd. trade name: YL983U, molecular weight: 310), 170 parts by weight of SiO_2 spherical particles having an average particle size of 1.6 μm and coated on its surface with a silane coupling agent (made by Adomatic Co., Ltd., trade name: CRS 1101-CE, the maximum size of the particles is not more than the thickness (15 μm) of inner layer copper pattern as mentioned below) and 1.5 parts by weight of a leveling agent (made by Sannopuko Co., Ltd., trade name: Perenol S4) are kneaded through three rolls and a viscosity thereof is subjected to 45,000~49,000 cps at 23±1℃.

② 6.5 parts by weight of an imidazole curing agent (made by Shikoku Kasei Co, Ltd. trade name: 2E4MZ-CN)

They are mixed to prepare a resin filler 10.

[0057]

D. Production of a printed circuit board

(1) As a starting material, there is used a copper-clad laminate formed by laminating a copper foil 8 of 18 μm in thickness onto each surface of a substrate 1 made from glass epoxy resin or BT (bismaleimide- triazine) resin and having a thickness of 1 mm (see Fig. 21). At first, the copper-clad laminate is subjected to an electroless plating treatment to form through-holes 9 and further the copper foil 8 is etched in a pattern according to the usual manner to form inner layer copper pattern 4 on both surfaces of the substrate 1.

[0058]

(2) The substrate provided with the inner layer copper pattern 4 and through-hole 9 is washed with water, dried and subjected to a redox treatment using an oxidizing aqueous solution of NaOH (10 g/l), $NaClO_2$ (40 g/l) and a reducing aqueous solution of NaOH (10 g/l) and $NaBH_4$ (6 g/l) to form a roughened layer 11 on the surfaces of the inner layer copper pattern 4 and the through-hole 9 (see Fig. 22).

[0059]

(3) The resin filler 10 is applied onto both surfaces of the substrate by means of a roll coater to fill between the conductor circuits 4 or in the through-holes 9 and dried at 70℃ for 20 minutes, and similarly, the resin filler 10 is filled between the conductor circuits 4 or in the through-holes 9 on the other side surface and then dried by heating at 70℃ for 20 minutes (see Fig. 23).

[0060]

(4) The one side surface of the substrate treated in step (3) is polished by a belt sander polishing using #600 belt polishing paper (made by Sankyo Rikagaku Co., Ltd.) in such a manner that the resin filler is not left on the surface of the inner layer copper pattern 4 and the land surface of the through-hole 9, and then buff-polished so as to remove scratches formed by the belt sander polishing. Such a series of polishing is applied to the other surface of the substrate.

Then, the substrate is heated at 100℃ for 1 hour, at 120℃ for 3 hours and at 180℃ for 7 hours to cure the resin filler 10 (see Fig. 24).

[0061]

Thus, the roughened layers 11 formed on the surface layer portion of the resin filler 10 filled in the through-hole 9 and the like and on the upper surface of the inner layer conductor circuits 4 are removed to smoothen both surfaces of the substrate, whereby there is obtained a wiring substrate wherein the resin filler

10 is strongly adhered to the side face of the inner layer conductor circuit 4 through the roughened layer 11 and the inner wall surface of the through-hole 9 is strongly adhered to the resin filler 10 through the roughened layer 11. That is, the surface of the resin filler 10 and the surface of the inner layer copper pattern 4 are the same plane in this step. Here, the curing resin filled has a Tg point of 155.6℃ and a linear thermal expansion coefficient of 44.5x 10^{-6}/℃.

[0062]
(5) A roughened layer (uneven layer) 11 of Cu-Ni-P alloy having a thickness of 2.5 μm is formed on the exposed surfaces of the inner layer conductor circuit 4 and the land of the through-hole 9 in step (4) and further a Sn layer having a thickness of 0.3 μm is formed on the surface of the roughened layer 11 (see Fig. 25, provided that the Sn layer is not shown).

The formation method is as follows. That is, the substrate is acidicly degreased and soft-etched and treated with a catalyst solution of palladium chloride and organic acid to give a Pd catalyst, which is activated and subjected to a plating in an electroless plating bath of pH=9 comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid, 0.1 g/l of surfactant and water to form the roughened layer 11 of Cu-Ni-P alloy on the upper surfaces of the copper conductor circuit 4 and land of through-hole 9. Then, Cu-Sn substitution reaction is carried out by immersing in a solution containing 0.1 mol/l of tin borofluoride and 1.0 mol/l of thiourea at a temperature of 50℃ and pH=1.2 to form the Sn layer of 0.3 μm on the surface of the roughened layer 11 (Sn layer is not shown).

[0063]
(6) The interlaminar insulating resin material of the item B (viscosity: 1.5 Pa·s) is applied onto both surfaces of the substrate treated in (5) by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60℃ for 30 minutes (pre-baking) to form an insulating layer 2a.

Further, the adhesive for electroless plating of the item A (viscosity: 7 pa·s) is applied onto the insulating layer 2a by means of a roll coater and left to stand at a horizontal state for 20 minutes and dried at 60℃ for 30 minutes (pre-baking) to form an adhesive layer 2b (see Fig. 26).

[0064]
(7) A photomask film depicted with black circles of 85 μm in diameter is closely adhered onto both surfaces of the substrate provided with the insulating layer 2a and the adhesive layer 2b in

step (6) and exposed to a super-high pressure mercury lamp at 500 mJ/cm^2. It is developed by spraying a DMTG solution and further exposed to a superhigh pressure mercury lamp at 3000 mJ/cm^2 and heated at 100℃ for 1 hour and at 50℃ for 5 hours (post-baking) to form an interlaminar insulating resin layer (two-layer structure) of 35 μm in thickness having openings of 85 μm in diameter (openings 6 for the formation of viaholes) with an excellent size accuracy corresponding to the photomask film (see Fig. 27). Moreover, the tin plated layer is partially exposed in the opening for viahole.

[0065]
(8) The substrate provided with the openings is immersed in 800 g/l of chromic acid at 70℃ for 19 minutes to dissolve and remove the epoxy resin particles existing on the surface of the adhesive layer 2b in the interlaminar insulating resin layer 2, whereby the surface of the interlaminar insulating resin layer 2 is roughened (depth: 3 μm) and thereafter the substrate is immersed in a neutral solution (made by Shipley) and washed with water (see Fig. 28).

Further, a palladium catalyst (made by Atotec Co., Ltd.) is applied to the roughened surface of the substrate to give a catalyst nucleus to the surface of the interlaminar insulating resin layer 2 and the inner wall surface of the opening 6 for viahole.

[0066]
(9) The substrate is immersed in an electroless copper plating bath having the following composition to form an electroless copper plated film 12 having a thickness of 0.6 μm on the full roughened surface (see Fig. 29).

[Electroless plating aqueous solution]

EDTA	150 g/l
copper sulfate	20 g/l
HCHO	30 g/l
NaOH	40 g/l
α , α -bipyridyl	80 mg/l
PEG	0.1 g/l

[Electroless plating condition]
liquid temperature of 70℃ for 30 minutes

[0067]
(10) A commercially available photosensitive dry film, is adhered to the electroless copper plated film 12 formed in step (9) and a mask is placed thereon and exposed to a light at 100 mJ/cm^2 and developed with 0.8% of sodium carbonate to form a plating resist 3 having a thickness of 15 μm (see Fig. 30).

[0068]

(11) Then, the non-resist forming portion is subjected to an electroless copper plating under the following conditions to form an electrolytic copper plated film 13 having a thickness of 15 μm (see Fig. 31).

[Electrolytic plating aqueous solution]

sulfuric acid	180 g/l
copper sulfate	80 g/l
additive (made by Atotec Japan Co., Ltd., trade name: Capalacid GL)	1 ml/l

[Electrolytic plating condition]

current density	1 A/dm^2
time	30 minutes
temperature	room temperature

[0069]

(12) After the plating resist 3 is peeled off with 5% KOH, the electroless plated film 12 beneath the plating resist 3 is dissolved and removed by etching with a mixed solution of sulfuric acid and hydrogen peroxide to form a conductor circuit 5 (including viahole) of 18 μm in thickness comprised of the electroless copper plated film 12 and the electrolytic copper plated film 13. Further, it is immersed in 800 g/l of chromic acid at 70℃ for 30 minutes to etch the surface of the adhesive layer for electroless plating between conductor circuits located at the portion not forming the conductor circuit by 1~2 μm to thereby remove the palladium catalyst remaining on the surface (see Fig. 32).

[0070]

(13) The substrate provided with the conductor circuits 5 is immersed in an electroless plating aqueous solution of pH=9 comprising 8 g/l of copper sulfate, 0.6 g/l of nickel sulfate, 15 g/l of citric acid, 29 g/l of sodium hypophosphite, 31 g/l of boric acid and 0.1 g/l of surfactant to form a roughened layer 11 of copper-nickel-phosphorus having a thickness of 3 μm on the surface of the conductor circuit 5 (see Fig. 33). In this case, the resulting roughened layer 11 has a composition ratio of Cu: 98 mol%, Ni: 1.5 mol% and P: 9.5 mol% as analyzed by EPMA (electro probe micro analyzer).

Further, Cu-Sn substitution reaction is carried out by immersing in a solution of 0.1 mol/l of tin borofluoride and 1.0 mol/l of thiourea at a temperature of 50℃ and pH=1.2 to form a Sn layer having a thickness of 0.3 μm on the surface of the roughened layer 11 (the Sn layer is not shown).

[0071]

(14) Steps (6)~(13) are repeated to further form upper layer

conductor circuits (including viaholes and alignment marks) to thereby produce a multilayer wiring substrate. However, Sn substitution is not conducted (see Figs. 34~39).

[0072]
(15) On the other hand, a solder resist composition is prepared by mixing 46.67 g of photosensitized oligomer (molecular weight: 4000) in which 50% of epoxy group in 60% by weight of cresol novolac epoxy resin (made by Nippon Kayaku Co., Ltd.) dissolved in DMDG is acrylated, 15.0 g of 80% by weight of bisphenol A-type epoxy resin (made by Yuka Shell Co., Ltd., trade name: Epikote 1001) dissolved in methyl ethyl ketone, 1.6 g of an imidazole curing agent (made by Shikoku Kasei Co., Ltd., trade name: 2E4MZ-CN), 3 g of a polyvalent acrylic monomer (made by Nippon Kayaku Co., Ltd., trade name: R604) as a photosensitive monomer, 1.5 g of a polyvalent acrylic monomer (made by Kyoeisha Kagaku Co., Ltd., trade name: DPE6A), 0.71 g of a dispersion type defoaming agent (made by Sannopuko Co., Ltd, trade name: S-65), 2 g of benzophenone (made by Kanto Kagaku Co., Ltd.) as a photoinitiator and 0.2 g of Micheler's ketone (made by Kanto Kagaku Co., Ltd.) as a photosensitizer and adjusting a viscosity to 2.0 Pa·s at 25℃.

Moreover, the measurement of the viscosity is carried out by means of a B-type viscometer (made by Tokyo Keiki Co., Ltd., DVL-B model) with a rotor No. 4 in case of 60 rpm or a rotor No. 3 in case of 6 rpm.

[0073]
(16) The above solder resist composition is applied onto both surfaces of the multilayer wiring substrate obtained in step (14) at a thickness of 20 μm. Then, the substrate is dried at 70℃ for 20 minutes and at 70℃ for 30 minutes and a photomask film of 5 mm in thickness depicted with circle pattern (mask pattern) is placed thereon and then exposed to an ultraviolet ray at 1000 mJ/cm^2 and developed with DMTG. Further, it is heated at 80℃ for 1 hour, at 100℃ for 1 hour, at 120℃ for 1 hour and at 150℃ for 3 hours to form a solder resist layer 14 (thickness; 20 μm) opened in the pad portion (including viahole and its lad portion, opening size: 200 μm).

[0074]
(17) Then, the substrate provided with the solder resist layer 14 is immersed in an electroless nickel plating aqueous solution of pH=5 comprising 30 g/l of nickel chloride, 10 g/l of sodium hypophosphite and 10 g/l of sodium citrate for 20 minutes to form a nickel plated layer 15 having a thickness of 5 μm in the opening portion. Further, the substrate is immersed in an electroless gold plating aqueous solution comprising 2 g/l of potassium gold cyanide, 75 g/l of ammonium chloride, 50 g/l of sodium citrate and

10 g/l of sodium hypophosphite at 93℃ for 23 seconds to form a gold plated layer 16 having a thickness of 0.03 μm on the nickel plated layer 15.

[0075]
(18) A solder paste is printed on the opening portion of the solder resist layer 14 and reflowed at 200℃ to form solder bumps 17 (solder body), whereby there is produced a printed circuit board having solder bumps (see Fig. 40).

[0076]
(Comparative Example)
A dry photo-resist is laminated on the substrate treated in steps (1), (2), (3), (4), (5), (6), (7) and (8) of Example 1, and exposed and developed to form a plating resist. Then, after step (9) of Example 1 is carried out, the plating resist is peeled and removed in the same manner as in step (12) and the whole surface of the conductor circuit is roughened by step (13) of Example 1. Thereafter, the formation of interlaminar insulating resin layer, roughening treatment, the formation of plating resist and electroless copper plating are carried out in the same manner as in Example 1, and after the plating resist is peeled and removed, a multilayer printed circuit board having solder bumps is produced by steps (15), (16), (17), (18) and (19) of Example 1.

[0077]
After IC chip is mounted onto each of the printed circuit boards of Examples and Comparative Example, heat cycle tests of 1000 cycles and 2000 cycles under conditions of -55℃ for 15 minutes, room temperature for 10 minutes and 125℃ for 15 minutes are carried out.
The evaluation of these tests are carried out by confirming occurrence of cracks in the printed circuit board by means of a scanning electron microscope after the test. Further, the peel strength is measured according to JIS-C-6481.

[0078]
As a result, the occurrence of cracks is not observed at about 1000 cycles in the Comparative Example and Examples 1~3, but observed at 2000 cycles in the Comparative Example.
The peel strength is equal or higher than that of the conductor circuit comprised of only an electroless plated film.
Thus, in the invention, the occurrence of cracks in the interlaminar insulating resin layer can be prevented while maintaining a practical peel strength.

[0079]

[Table 1]

	1000 cycles	2000 cycles	Peel strength
Example 1	None	None	1.2kg/cm
Example 2	None	None	1.0kg/cm
Example 3	None	None	1.0kg/cm
Comparative Example	None	Yes	0.9kg/cm

[0080]
[Effect of the Invention]

As explained above, according to the invention, it is possible to prevent the occurrence of cracks in the heat cycle and connection reliability can be improved while preventing the degradation of the peel strength.

[Brief Description of the Drawings]
[Fig. 1]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 2]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 3]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 4]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 5]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 6]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 7]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 8]

A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 9]

A flowchart showing the production of a multilayer printed

circuit board according to the invention.
[Fig. 10]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 11]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 12]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 13]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 14]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 15]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 16]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 17]
A flowchart showing the production of a multilayer printed circuit board according to the invention.
[Fig. 18]
A structure enlarged view of a multilayer printed circuit board according to the invention.
[Fig. 19]
A structure enlarged view of a multilayer printed circuit board according to the invention.
[Fig. 20]
A triangular diagram showing a composition of copper-nickel-phosphorus roughened layer.
[Fig. 21]
A flowchart showing each production of a multilayer printed circuit board according to the invention.
[Fig. 22]
A flowchart showing each production of a multilayer printed circuit board according to the invention.
[Fig. 23]
A flowchart showing each production of a multilayer printed circuit board according to the invention.
[Fig. 24]
A flowchart showing each production of a multilayer printed circuit board according to the invention.
[Fig. 25]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 26]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 27]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 28]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 29]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 30]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 31]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 32]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 33]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 34]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 35]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 36]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 37]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 38]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 39]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Fig. 40]

A flowchart showing each production of a multilayer printed circuit board according to the invention.

[Explanation of the Signs]

1	substrate
2	interlaminar insulating resin layer (adhesive layer for electroless plating)
2a	insulating layer
2b	adhesive layer
3	plating resist
4	inner layer conductor circuit (inner layer copper pattern)
5	outer layer conductor circuit (outer layer copper pattern)
6	opening for viahole
7	viahole
8	copper foil
9	through-hole
10	filling resin
11	roughened layer
12	electroless copper plated film
13	electrolytic copper plated film
14	solder resist layer
15	nickel plated layer
16	gold plated layer
17	solder bump

[Name of the Document] Abstract

[Subject]

To prevent the occurrence of cracks in the interlaminar insulating layer caused in the heat cycle without the degradation of the peel strength.

[Solution]

A multilayer printed circuit board formed with an interlaminar insulating layer on a conductor circuit of a wiring substrate, characterized in that the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit.

[Selected Drawing] None